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**[4657]-546****S.E. (E&TC/Electronics) (Second Semester) EXAMINATION, 2014****INTEGRATED CIRCUITS****(2012 PATTERN)****Time : Two Hours****Maximum Marks : 50**

**N.B. :—** (i) Answer Q. 1 or Q. 2, Q. 3 or Q. 4, Q. 5 or Q. 6 and  
Q. 7 or Q. 8.

(ii) Neat diagrams must be drawn wherever necessary.

(iii) Figures to the right indicate full marks.

(iv) Use of calculator is allowed.

(v) Assume suitable data, if necessary.

**1. (a)** Define the following characteristics of practical op-amp : [6]

(i) Input offset voltage

(ii) CMMR

(iii) PSSR

(iv) Slew rate.

P.T.O.

- (b) What is slew rate ? What are its causes ? Derive its expression for maximum frequency of operation for a desire output swing in terms of slew rate. [6]

*Or*

2. (a) Justify, how constant current source is used in place of  $R_E$  to improve the CMRR for a differential amplifier. [6]
- (b) What is need for frequency compensation ? State and explain Pole—Zero compensation method of frequency compensation. [6]
3. (a) Why basic Integrator is needed to be modified ? Draw the circuit diagram of Practical Integrator along with frequency response and explain its operation. [6]
- (b) List important characteristics of Comparator ? What are the advantages of Schmitt trigger over Comparator ? [6]

*Or*

4. (a) Draw circuit diagram of Three op-amp Instrumentation Amplifier and write its output equation. [6]
- (b) Design a Schmitt trigger for  $U_{TP} = 3V$  and  $L_{TP} = -2V$  with general purpose op-amp 741. Assume  $V_{CC} = +/-12V$ . Draw detailed diagram with designed values. [6]

5. (a) Draw a neat schematic of Voltage Controlled Oscillator (VCO) using Op-amp. Derive the expression for output frequency. [6]
- (b) With the help of a neat block diagram, explain operation of Phase Locked Loop (PLL). Define the term “Lock Range” and “Capture Range”. [7]

*Or*

6. (a) Explain Voltage to Current Converter with grounded load using Op-amp and give its applications. [6]
- (b) Define “Lock Range”, “Capture Range” and “Pull-in time” and explain the transfer characteristics of Phase Locked Loop (PLL). [7]
7. (a) Draw the circuit diagram of Voltage mode R—2R ladder Digital to Analog converter (DAC) and explain its working. [7]
- (b) Calculate output frequency ' $f_o$ ', Lock range ' $\Delta f_L$ ', Capture range ' $\Delta f_C$ ' of a PLL, If  $R_T = 1 \text{ k}\Omega$ ,  $C_T = 0.1 \text{ }\mu\text{f}$  and filter capacitor  $C = 10 \text{ }\mu\text{f}$ . Assume  $V = 20 \text{ V}$ . [6]

*Or*

8. (a) Explain successive approximation type ADC with neat block diagram. An 8-bit ADC output all 1's, when  $V_i = 5.1$  V. Find its : [8]
- (i) Resolution
- (ii) Digital output, when  $V_i = 1.28$  V.
- (b) Explain various power supply performance parameters. [5]

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